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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/542,671 | 12/28/2005 | Magnus Bengtsson | P17807-US2 | 1680 |

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| EXAMINER | |
|---|---|
| MALEK, LEILA | |

| ART UNIT | PAPER NUMBER |
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| 2611 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/542,671 | BENGTSSON ET AL. | |
| | Examiner | Art Unit | |
| | LEILA MALEK | 2611 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *07 October 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-19 and 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2009* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/07/2009 has been entered.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-19 and 21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. As to claims 1 and 10, Applicant in invention's disclosure fails to disclose "comparing the original despread data symbol represented by the first number of bits to the truncated data symbol represented by the second number of bits obtained from the original despread data symbol represented by the first number of bits; if the value of the original despread data symbol represented by the first number of bits is larger than the highest value that can be represented by the truncated data symbol represented by the

second number of bits, then replacing each such truncated data symbol represented by second number of bits with said highest value that can be represented by the second number of bits; or if the value of the original despread data symbol represented by the first number of bits is less than the lowest value that can be represented by the truncated data symbol represented by the second number of bits; then replacing each such truncated data symbol with said lowest value that can be represented by the second number of bits." In invention's disclosure, pages 11 and 12, Applicant does not show such a comparison. Applicant on page 11, states that "The truncated and saturated values $t_I$ and $t_Q$ are computed from the values $g_I$ and $g_Q$ by extracting the $N_t$ least significant bits, if this equals $g_I$ and $g_Q$." However, it is not clear if "this" is referring to the least significant bits or it refers to the truncated and saturated values. Furthermore, if we assume that "this" refers to the truncated and saturated values, it is not clear how the truncated values can be equal to the original signal values. Finally, it is not clear if term "value" represents the number of bits or it refers to a bit value (e.g. if the bit is 1 or 0). Claims 2-9, 11-19, and 21 are rejected as well, because they depend on claims 1 or 10, respectively. In view of the 35 U.S.C. 112, first paragraph rejection, no patentable weight has been given to the comparing steps of claims 1 and 10. In light of specification, the limitations regarding the comparing steps have been interpreted as having overflow condition in the system.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-7, 10-16, 19, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's background of invention, in view of Mathe (US 2002/0051502).

As to claims 1 and 10, Applicant in the background of invention discloses a method/apparatus for receiving radio signals in a receiver for a digital wireless communications system (see pages 2, 3, and 4), the method comprising the steps of: level adjusting a received radio signal by an automatic gain control (see page 3, line 5 – line 33); and despreading the level adjusted signal in a RAKE unit having a number of fingers (see the description of Fig. 3, on page 10, lines 23 – page 4, line 5), thus providing a number of original despread data symbols, each despread data symbol being represented by a first number of bits (see page 11, line 5), maintaining each original despread data symbol represented by the first number of bits in a memory (see page 11, lines 19-21), and level adjusting the despread data symbols provided from the RAKE unit (see page 11, lines 14-17). Applicant in the background of invention discloses all the subject matters claimed in claims 1 and 10, except that the method further comprises the steps of: obtaining from each original despread data symbol represented by the fist number of bits, a truncated data symbol represented by a second number of bits, the second number of bits being the least significant bits of the first number of bits; maintaining each truncated data symbol represented by the second number of bits in a memory; saturating the truncated data symbols represented by the

second number of bits to obtain saturated data symbols by replacing the second number of bits by a value determined as follows: comparing the original despread data symbol represented by the first number of bits to the truncated data symbol represented by the second number of bits obtained from the original despread data symbol represented by the first number of bits; if the value of the original despread data symbol represented by the first number of bits is larger than the highest value that can be represented by the truncated data symbol represented by the second number of bits, then replacing each such truncated data symbol represented by second number of bits with said highest value that can be represented by the second number of bits; or if the value of the original despread data symbol represented by the first number of bits is less than the lowest value that can be represented by the truncated data symbol represented by the second number of bits; then replacing each such truncated data symbol with said lowest value that can be represented by the second number of bits; obtaining a new despread data symbol by replacing the second number of bits as the least significant bits with, as the case may be, the highest value that can be represented by the second number of bits, or lowest value that can be represented by the second number of bits, as determined in the saturating and comparing steps. Mathe discloses a method for receiving radio signals in a receiver of a communication system (see Fig. 6 and paragraph 0015). Mathe further discloses obtaining from each original received data symbol represented by the fist number of bits, a truncated data symbol represented by a second number of bits (see Fig. 1, block 40 and paragraph 0037), the second number of bits being the least significant bits of the first number of bits (see

paragraph 0037, 5 LSBs are truncated); saturating the truncated data symbols represented by the second number of bits to obtain saturated data symbols (see Fig. 1, block 42 and Fig. 4, block 100, adders 104,118, and paragraph 0064) by replacing the second number of bits by a value determined as follows (see paragraph 0064): determining if there is a bit overflow (see paragraph 0064); if the number of bits is larger than the highest value that can be represented by the truncated data symbol, then replacing each such truncated data symbol represented by second number of bits with said highest value that can be represented by the second number of bits (see paragraph 0064); or if the number of bits is less than the lowest value that can be represented by the truncated data symbol represented, then replacing each such truncated data symbol with said lowest value that can be represented by the second number of bits (see paragraph 0064); obtaining a new despread data symbol by replacing the second number of bits as the least significant bits with, as the case may be, the highest value that can be represented by the second number of bits, or lowest value that can be represented by the second number of bits, as determined in the saturating step (see Fig.4, the output of adder 104); level adjusting the new data symbols (see Fig. 1, block 22). Mathe does not disclose that the despread data has been truncated because despreading has been performed by the sample rate conversion circuit 182 (see paragraph 0073), however, the location of despreader in the circuit is a matter of design choice and it would have been obvious to one of ordinary skill in the art at the time of invention to alternatively place the despreader prior to the truncation unit to meet the design requirements of the system. Furthermore, Mathe does

not expressly disclose maintaining each truncated data symbol represented by the second number of bits in a memory. However, it would have been extremely well known in the art at the time of invention to save the data (truncated data) in a memory for further processing. It would have been obvious to one of ordinary skill in the art at the time of invention to modify Applicant's background of invention as suggested by Mathe to reduce the number of bits and as the result prevent overflowing of the decoder.

As to claims 2 and 11, Applicant in the background of invention discloses that the step of level adjusting the despread data symbols provided from the RAKE unit comprises the step of measuring the level (interpreted as power) of the despread data symbols (see page 3, lines 23-24).

As to claims 3 and 12, Mathe further shows measuring the level of the saturated data symbols (see paragraph 0046, Figs. 1 and 6, baseband processor 24 and memory 26); and then level adjusting the received data symbols based on the measured level of the saturated data symbols (see blocks 186, 188, 182, 24, and feedback from block 24 to gain stepping circuit 186). It would have been obvious to one of ordinary skill in the art at the time of invention, to modify Applicant's background of invention, by using the teaching of Mathe and adjust the level of the despread data symbols provided from the rake unit based on the measured level of the saturated data symbols to shrink the size of the circuit by using the truncated and saturated bits instead of the entire number of bits.

As to claims 4 and 13, Applicant in the background of invention discloses that that level adjusting of the despread data symbols is performed by adjusting a reference value (or factor) of the automatic gain control (see page 3, lines 21-26).

As to claims 5 and 14, Applicant in the background of invention discloses that level adjusting of the despread data symbols is performed by adjusting the level of each despread data symbol individually in dependence of that despread data symbol (see page 3, last paragraph).

As to claims 6 and 15, Applicant's background of invention and Mathe do not expressly disclose level adjusting based on the largest of an in-phase and quadrature phase components of the despread data symbols. However, it would have been obvious to one of ordinary skill in the art at the time of invention to perform the adjustment based on the largest I and Q values to reduce the power consumption.

As to claim 7 and 16, Applicant in the background of invention discloses level adjusting based on the data symbols averaged over time (see page 3, lines 21-24).

As to claim 19, Applicant in the background of invention discloses that the receiver is a WCDMA receiver (see page 3, last paragraph).

As to claim 21, document WO 00/69086 (i.e. the background of invention) discloses that the communication system is software implemented (see the abstract) system. It would have been extremely recognizable to one of ordinary skill in the art at the time of invention to use a computer (or a processor on a computer) to run the software programs disclosed by the background of invention and transfer orders to different parts of the communication system.

4. Claims 8 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's background of invention and Mathe, further in view of Drake et al. (hereafter, referred as Drake) (US 6,366,395).

As to claims 8 and 17, Applicant's background of invention and Mathe disclose all the subject matters claimed in claims 1 and 10, except that the level adjusting is performed using a proportional-integral control algorithm. Drake discloses an amplifier with a power measurement circuit for measuring the input and output power of the amplifier (see the abstract). Drake further discloses that the desired or target output power calculated by the unit 70 is provided to the error calculation circuit 24 which calculates the error between the target output power and the measured output power from the amplifier (see column 5, lines 5-15). Drake shows that the processing applied to the error signal 76 is proportional and integral control, to provide the desired control signal so that the amplifier can report rapidly to a required change in pump power (see Fig. 5, and column 5, lines 12-16). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Applicant's background of invention and Mathe as suggested by Drake to rapidly adjust the level of the signal.

5. Claims 9 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's background of invention and Mathe, further in view of Haddad et al. (hereafter, referred as Haddad) (US 4,715,063).

As to claims 9 and 18, Applicant's background of invention and Mathe disclose all the subject matters claimed in claims 1 and 10, except that level adjusting is performed by selecting one of two different adjustment levels. Haddad discloses a

communication system, wherein transmit and receive signal detectors 206 and 207 include substantially identical circuit blocks 208-245. Both detectors 206 and 207 are comprised of conventional circuit blocks including at least a gain adjust circuitry 208. The gain adjust circuitry 208 varies the gain between two pre-selected levels depended on the binary state of detector control signal 224 (225 for detector 207). The logarithmic amplifier 240 extends the dynamic range of the detectors 206 and 207 due to its amplification characteristic (see column 5, lines 30-42). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Applicant's background of invention and Mathe as suggested by Haddad to adjust the gain of the received signal quicker (see column 6, last paragraph).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LEILA MALEK whose telephone number is (571)272-8731. The examiner can normally be reached on 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Leila Malek
Examiner
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